



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Terletzki et al.

Art Unit: 2816

Serial No.: 09/659,872

Examiner: Minh Nguyen

Filed: Sept. 13, 2000

Docket: 00-P-7882 US

For: Level-Shifting Circuitry Having "High" Output Impedance During Disable Mode

#10/elt
K
Drawing
Changes
5/6/02
Shm H

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)

I hereby certify, that on this date, this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231.

Nancy J. Todd

Date

04/03/02

Amendment under 37 C.F.R. §1.111

Commissioner for Patents
Washington, D.C. 20231

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Dear Sir:

The following remarks are offered in response to the Examiner's Office Action dated December 5, 2001. They are respectfully submitted as a full and complete response to that Action. Marked versions of changes to specification and claims are attached as Appendix I and II, respectively.

Please amend the above-referenced application as follows:

In the Drawings:

Please replace Figures 1-2 with the redlined copies that are attached.

04/16/2002 CVD111 00000118 192179 09659872

01 FC:102 252.00 CH
02 FC:103 432.00 CH

04/16/2002 CVD111 00000118 192179 09659872

03 FC:115 110.00 CH